29.7 A Voltage Regulator for Subthreshold Logic with Low Sensitivity to Temperature and Process Variations

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In energy-constrained systems low-power design is essential for extending battery and system lifetime. Recently, subthreshold circuits are becoming popular in emerging embedded applications, such as wireless sensor networks, where the key metric is energy dissipation rather than high-speed performance [1]. Because of the exponential I-V characteristic of a MOS transistor in the subthreshold region [2], the performance of subthreshold digital circuits is very sensitive to temperature and threshold voltage variations [3,4]. The idea that forms the foundation for this paper is to compensate such sensitivity by providing to the subthreshold circuit an ad hoc supply voltage that is dependent on temperature and on the particular occurrence of process parameters. We present a voltage regulator providing a supply voltage V_{DD} that makes the propagation delay of a subthreshold digital circuit almost insensitive to temperature and process variations. The block diagram is shown in Fig. 29.7.1. The core of the voltage regulator is the current reference circuit that generates a current I_{REF} proportional to the product of the generated supply voltage V_{DD} and the reference voltage V_0. Since M_{N1} and M_{N2} are identical, the operational amplifier ensures that I_0 is equal to I_{REF}. A series voltage regulator provides the regulated voltage V_{REG}, which is equal to V_{DD}. If a CMOS inverter with a PMOS identical to M_{P2} is connected to V_{REG}, the load capacitance will be charged with the current I_{REF} when the PMOS conducts. The current reference circuit is shown in Fig. 29.7.2. The two transistors M_1 and M_2 work in the triode region. The two operational amplifiers A_1 and A_2 impose the reference voltage $V_0 = V_{REF} / \gamma$ (in general $0 < \gamma < 1$) between the drains and sources of M_1 and M_2. By using the equation for the I-V characteristic of a MOS transistor in the triode region, the current I_{REF} is given by $I_{REF} = 2k(1-\alpha)V_{DD}V_{REF} / \gamma$ (where α is chosen so that $0 < \alpha < 1$). The voltage reference generator is shown in Fig. 29.7.3 and consists of a circuit that generates a bias current I_2 as independent as possible of the supply voltage; I_2 is then injected into an active load (M_7 through M_{10}) to generate the reference voltage [5]. In the current generator of Fig. 29.7.3, M_{12} and M_{13} operate in the subthreshold region, while M_3 and M_4 are in the saturation region. The active load used to generate the reference voltage consists of two NMOS transistors, M_7 and M_8, that are 3.3V NMOS devices with threshold voltage $V_{thL} = 0.45$ V biased by I_2, and a voltage divider formed by M_9 and M_{10}, which are 5V NMOS devices with threshold voltage $V_{thH} = 0.75$ V. The propagation delay of a CMOS inverter supplied by the proposed voltage regulator can be written as

$$t_p = \frac{C}{4\mu C_{ox} W / L(1-\alpha)V_{REF} / \gamma}, \quad (1)$$

where C is the load capacitance, μ is the carrier mobility in the channel, C_{ox} is the oxide capacitance and W and L are the channel width and length, respectively. Since α and γ are partition coefficients, they can be considered to a first approximation independent of temperature and process variations. To obtain a zero temperature coefficient for t_p, the temperature coefficient of the reference voltage must be $-\mu_T V_{REF} / T$, where μ_T is mobility temperature exponent. By imposing the previous condition, we find the value of $(W_{10}/L_{10})/(W_9/L_9)$ that minimizes the sensitivity to temperature variations. Subthreshold digital circuits are strongly affected by process variations because of the exponential dependence of the drain current on the threshold voltage shift, and therefore exhibit huge sensitivity to process variations. Monte Carlo simulations predict a relative standard deviation of the propagation delay of a subthreshold CMOS inverter larger than 300%. According to (1), the variance of t_p for our voltage regulator depends upon the variances of the mobility and of the reference voltage V_{REF} if we assume that the process variations on W and L negligible (large W and L). The voltage regulator has been implemented in a 0.35µm CMOS process. The die micrograph is shown in Fig. 29.7.4. A CMOS inverter has been supplied by the voltage regulator and by a constant voltage, whose value has been chosen in such a way that, at room temperature, the rise times of the inverters are equal in the two cases. Figure 29.7.5 shows the rise times of both inverters as a function of temperature. When the regulator is used, the temperature coefficient of the rise time is 114ppm/°C. In the case of a constant supply voltage the temperature coefficient is 5.5%/°C. In order to test the sensitivity to process variations, the rise times of both inverters have been measured for 20 different samples from the same batch and the results are shown in Fig. 29.7.6. Experimental results show that $3\sigma_{tp}/t_p$ is 14.81% in the case of the inverter supplied by the voltage regulator (Monte Carlo simulations account also for inter-batch variations and predict a larger $3\sigma_{tp}/t_p$ of 21.8%) and 368.5% with a constant supply voltage.

The same measurements have been repeated with a ring oscillator and the oscillation frequency has been measured both with a constant supply voltage and with our supply voltage regulator. When the regulator is used, the TC of the oscillation frequency is 185ppm/°C. The oscillation frequency as a function of temperature is shown in Fig. 29.7.7 (left). In the case of a constant supply voltage, the TC of the frequency is 20.5%/°C; that is, more than 1000 times larger. The ring oscillator, in both cases, has been tested in 20 different samples. Experimental results, presented as histograms in Fig. 29.7.7 (right) show that $3\sigma_{fosc}/f_{osc}$ is 15.6% for the ring oscillator supplied by the voltage regulator (Monte Carlo simulations predict $3\sigma_{fosc}/f_{osc}$ = 21.6%) and 406% with a constant supply voltage. The supply voltage range that ensures correct operation of the voltage regulator is from 1.8 to 4.3V. The minimum supply current measured at the minimum supply voltage and at 0°C is 2.9µA and the maximum supply current measured at the maximum supply voltage and at 80°C is 3.4µA.

The voltage regulator also ensures a very small sensitivity of the digital subthreshold circuit to variations in the unregulated supply voltage. For the CMOS inverter supplied by the voltage regulator, when the supply voltage varies from its minimum to its maximum value, the rise time varies by 2.87%, which yields a line sensitivity of 1.2%/V. In the case of the ring oscillator, when the unregulated supply voltage varies from its minimum to its maximum value, the oscillation frequency varies by 1.9%, leading to a line sensitivity of 0.77%/V. The area occupied by the chip is 0.44mm².

Acknowledgments:
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[1] H. Soeleman and K. Roy, "Ultra-Low Power Digital Subthreshold Logic Circuits," *Proc. Int'l. Symp. Low Power Electronics and Design*, pp. 94-96, 1999.
[2] Y. Taur and T.H. Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, 1998, pp. 126-128.
[3] H. Soeleman, K. Roy and B.C. Paul, "Robust Subthreshold Logic for Ultra-Low Power Operation," *IEEE T. VLSI Systems*, pp. 90-99, Jan., 2001.
[4] B. Zhai et al., "Analysis and Mitigation of Variability in Subthreshold Design, "*Proc. Int'l. Symp. Low Power Electronics and Design*, pp. 20-25, 2005.
[5] G. De Vita and G. Iannaccone, "A 300 nW, 12 ppm/°C Voltage Reference in Digital 0.35 µm CMOS Process," *Symp. VLSI Circuits*, pp. 81-82, 2006.

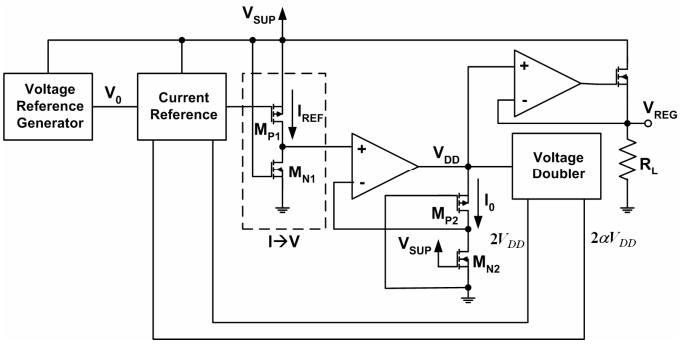

Figure 29.7.1: Block diagram of the regulator.

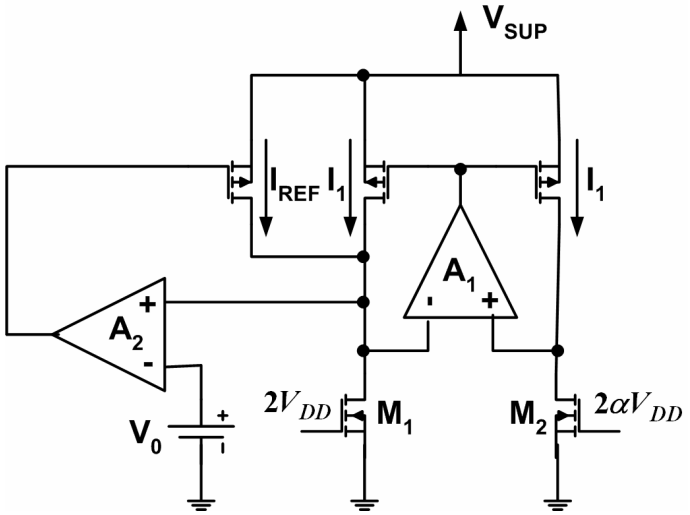

Figure 29.7.2: Schematic of the current reference circuit.

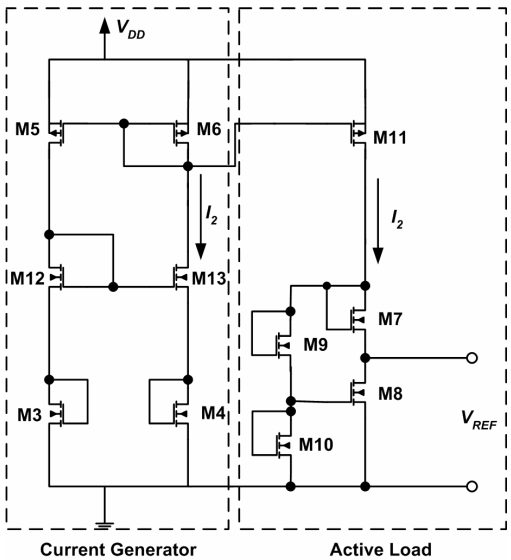

Figure 29.7.3: Schematic of the voltage reference generator.

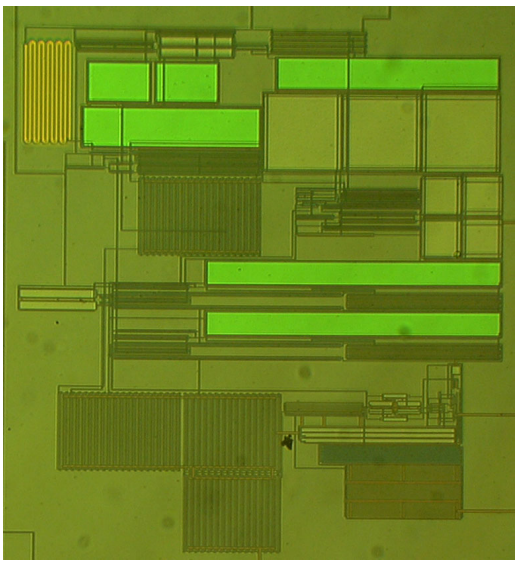

Figure 29.7.4: Chip micrograph (die core).

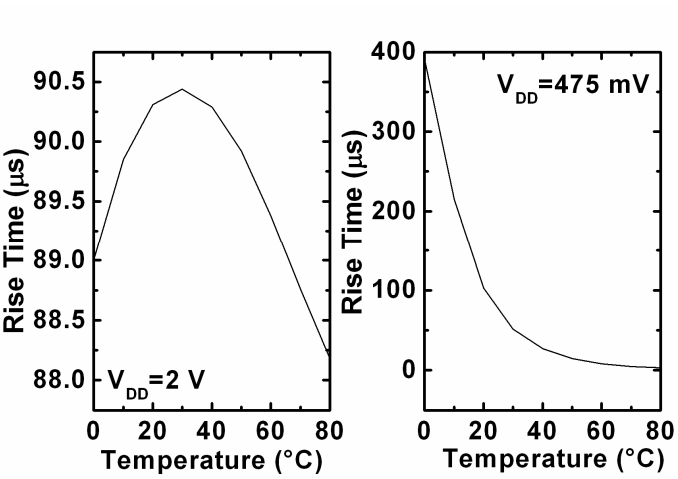

Figure 29.7.5: Rise time of the inverter versus temperature.

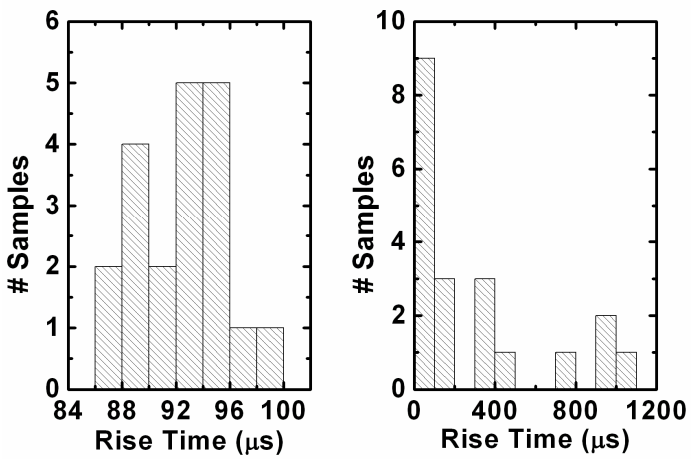

Figure 29.7.6: Sensitivities of the rise times of the inverters to process variations.

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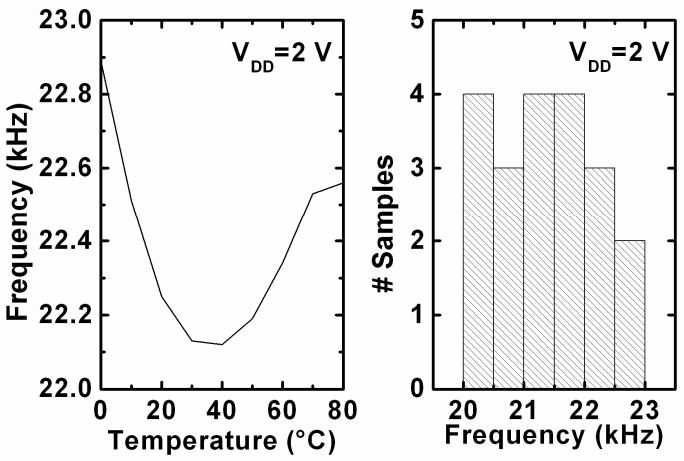

Figure 29.7.7: Sensitivity of the oscillation frequency to temperature (left) and process variations (right).

